What is claimed is:

1. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

Sub a7

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

2. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the high dielectric layer comprises a material selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, and (Pb, La)(ZrTi)O_3.

3. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the plate electrode and the storage electrode comprises a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

4. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first temperature is between 600°C and 900°C.

5. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the second temperature is between 100°C and 600°C.

6. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed separately or in-situ.

7. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed in a furnace or a rapid vacuum thermal annealing apparatus.

8. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the high dielectric layer.

Sub C27

9. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the plate electrode.

10. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

11. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising forming an interdielectric layer over the plate electrode.

~~12. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first and second post-annealing steps are performed after the step of forming the interdielectric layer.~~

13. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

14. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.

15. A method for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature, after forming one of the high dielectric layer, the plate electrode, and the interdielectric layer; and

Sub a47

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

16. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the high dielectric layer comprises a material selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, and (Pb, La)(ZrTi)O_3.

17. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the plate electrode and the storage electrode comprise a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

18. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the first temperature is between 600°C and 900°C.

19. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the second temperature is between 100°C and 600°C.

20. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, further comprising performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.